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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,602	04/16/2004	Yee-Chia Yeo	TSM03-0847	1196

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EXAMINER

RAYMOND, BRITTANY L

ART UNIT	PAPER NUMBER
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1756

MAIL DATE	DELIVERY MODE
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10/02/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/826,602	Applicant(s) YEO ET AL.	
	Examiner Brittany Raymond	Art Unit 1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 July 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 23-34, 37-54, 56 and 58-65 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 23-34, 37-54, 56 and 58-65 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 July 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 23-30, 33, 34 and 60-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirayama (U.S. Patent Publication 2006/0141400) in view of Meagley (U.S. Patent Publication 2005/0084794).

Hirayama ('400) discloses an immersion exposure process comprising: applying a resist composition onto a substrate (Paragraph 0137), immersing the substrate in a refractive index liquid and exposing the substrate with light through a mask pattern and the liquid to reach the resist layer (Paragraphs 0141 and 0142), as recited in claims 23, 30 and 61 of the present invention. Example 1 discloses that a resist film having a thickness of 150 nm can be formed on the substrate (Paragraph 0157), as recited in claim 23 of the present invention. Hirayama also discloses that the refractive index

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liquid can include water (Paragraph 0145), as recited in claims 24 and 62 of the present invention. Hirayama states that the light used in the exposure can be an ArF excimer laser, a KrF excimer laser, an F₂ excimer laser, etc. (Paragraph 0144), which is known by one of ordinary skill in this art to have a wavelength of less than 450 nm, as recited in claims 25 and 63 of the present invention. Hirayama discloses that the exposed resist film can be developed using an alkaline developer solution (Paragraph 0148), as recited in claim 33 of the present invention. Example 1 discloses that the developer can be tetramethylammonium hydroxide (Paragraph 0160), as recited in claims 34 and 65 of the present invention. Hirayama also discloses that a protective film can be formed over the resist film (Paragraph 0140), or in other words, that the upper portion of the resist film is treated, as recited in claim 61 of the present invention. Hirayama ('400) states in Example 1 that the protective film was formed by mixing a certain composition of materials together, spin coating this onto the resist film, and heating the substrate until the protective film has a certain thickness (Paragraph 0158), as recited in claim 60 of the present invention.

Hirayama ('400) fails to disclose that the photoresist layer completely diffuses with the immersion fluid prior to exposure, that the photoresist can be a chemically amplified photoresist and that the optical surface can comprises silicon oxide or calcium fluoride.

Meagley discloses an immersion lithography process comprising: providing a substrate with a photoresist layer, placing an index-matching liquid between the photoresist and a last lens for illuminating the photoresist, and incorporating additives

into the photoresist to promote diffusion of the photoresist into the index-matching liquid in order for the photoresist to patterned more effectively (Paragraph 0037), as recited in claims 23 and 29 of the present invention. Meagley also discloses that chemically amplified photoresists are often used in this process (Paragraph 0020), as recited in claims 28 and 64 of the present invention. Meagley states that the last lens can be made of silicon oxide or calcium fluoride (Paragraph 0023), as recited in claims 26 and 27 of the present invention.

It would have been obvious to one of ordinary skill in this art, at the time of invention by applicant, to have allowed the photoresist layer and the immersion fluid to diffuse together, as suggested by Meagley, in the process of Hirayama ('400) because Meagley teaches that this provides for improved performance of the photoresist during the patterning process. It also would have been obvious to one of ordinary skill in the art to have used a chemically amplified resist, as suggested by Meagley, in the process of Hirayama ('400) because Meagley teaches that chemically amplified photoresists can work well in immersion lithography processes. Finally, it would have been obvious to one of ordinary skill in this art to have used silicon oxide or calcium fluoride for the optical surface, as suggested by Meagley, in the process of Hirayama ('400) because Meagley teaches that this type of material does not react with the immersion liquid used and works well with the type of exposure light used in the present invention.

3. Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirayama (U.S. Patent Publication 2006/0141400) in view of Meagley (U.S. Patent

Publication 2005/0084794), as applied to claims 23-30, 33, 34 and 64 above, and further in view of Levinson (U.S. Patent Publication 2005/0037269).

The teachings of Hirayama ('400) and Meagley have been discussed in paragraph 2 above.

Hirayama ('400) and Meagley fail to disclose that there is a stage underlying the semiconductor structure and that the stage is immersed in the immersion fluid.

Levinson discloses an immersion lithography apparatus comprising a stage upon which the wafer to be patterned is mounted (Paragraph 0018), as recited in claim 31 of the present invention. Levinson also discloses in Figure 1 that the wafer region is immersed in the immersion fluid. It would be obvious to immerse the stage underlying the wafer in the immersion fluid since the stage is part of the wafer region, as recited in claim 32 of the present invention.

It would have been obvious to one of ordinary skill in this art, at the time of invention by applicant, to have included a stage underneath the semiconductor wafer and immersed the stage in the immersion fluid, as suggested by Levinson, in the process of Hirayama ('400) and Meagley because Levinson teaches that a stage is needed to hold the semiconductor substrate and move it around in order to pattern the substrate, and immersing the whole stage allows for the pattern to be formed properly

4. Claims 37-43, 46-50, 53 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirayama (U.S. Patent Publication 2006/0141400) in view of Meagley (U.S. Patent Publication 2005/0084794), as applied to claims 23-30, 33, 34 and 64 above, and further in view of Chang (U.S. Patent Publication 2005/0123863).

The teachings of Hirayama ('400) and Meagley have been discussed in paragraph 2 above. Hirayama ('400) teaches the recitations of dependent claims 38, 39, 43 and 46-48 of the present invention. Meagley teaches the recitations of dependent claims 40-42 of the present invention.

Hirayama ('400) and Meagley fail to disclose that the semiconductor wafer is processed after patterning the photoresist layer, that there is a layer of material deposited on the substrate before the photoresist is deposited and that this layer is further processed after patterning the photoresist, and that the layer of material is a conductive layer or a dielectric layer.

Chang discloses an immersion lithography process comprising: providing a material layer, forming a photoresist layer on the material layer, forming a protective layer on the photoresist layer, performing an immersion exposure step to pattern the photoresist layer, developing the photoresist layer, and performing an etching or an ion implantation process to process the material layer by using the photoresist layer as a mask (Paragraphs 0020-0023 and 0027-0028), as recited in claims 37, 46 and 49 of the present invention. Chang states that the material layer can be a dielectric layer or an electrically conductive layer (Paragraph 0020), as recited in claims 50 and 53 of the present invention.

It would have been obvious to one of ordinary skill in this art, at the time of invention by applicant, to have placed a conductive or dielectric layer over the substrate prior to the photoresist in order for it to be processed following patterning of the photoresist, as suggested by Chang, in the process of Hirayama ('400) and Meagley

because Chang teaches that these types of layers are needed in order to form a semiconductor device properly.

5. Claims 44 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirayama (U.S. Patent Publication 2006/0141400), Meagley (U.S. Patent Publication 2005/0084794) and Chang (U.S. Patent Publication 2005/0123863), as applied to claims 37-43, 46-50, 53 and 60 above, and further in view of Levinson (U.S. Patent Publication 2005/0037269).

The teachings of Hirayama ('400), Meagley and Chang have been discussed in paragraphs 2 and 4 above.

Hirayama ('400), Meagley and Chang fail to disclose that there is a stage underlying the semiconductor structure and that the stage is immersed in the immersion fluid.

Levinson discloses an immersion lithography apparatus comprising a stage upon which the wafer to be patterned is mounted (Paragraph 0018), as recited in claim 44 of the present invention. Levinson also discloses in Figure 1 that the wafer region is immersed in the immersion fluid. It would be obvious to immerse the stage underlying the wafer in the immersion fluid since the stage is part of the wafer region, as recited in claim 45 of the present invention.

It would have been obvious to one of ordinary skill in this art, at the time of invention by applicant, to have included a stage underneath the semiconductor wafer and immersed the stage in the immersion fluid, as suggested by Levinson, in the processes of Hirayama ('400), Meagley and Chang because Levinson teaches that a

stage is needed to hold the semiconductor substrate and to move it around, in order to pattern the substrate, and immersing the whole stage allows for the pattern to be formed properly.

6. Claims 51, 52, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirayama (U.S. Patent Publication 2006/0141400), Meagley (U.S. Patent Publication 2005/0084794) and Chang (U.S. Patent Publication 2005/0123863), as applied to claims 37-43, 46-50, 53 and 60 above, and further in view of Cheng (U.S. Patent 7176522).

The teachings of Hirayama ('400), Meagley and Chang have been discussed in paragraphs 2 and 4 above.

Hirayama ('400), Meagley and Chang fail to disclose that the conductive layer can be etched into gate electrodes with the gate electrodes having a minimum dimension of 50 nm or less, and that trenches can be formed in the dielectric layer, with the trenches being filled with a conductor.

Cheng discloses a process for forming a semiconductor device comprising forming gate electrodes with a height of 10 to 200 nm (Column 3, Lines 24-33), as recited in claims 51 and 52 of the present invention. Cheng also discloses that source/drain regions may be formed in the substrate by etching recesses in the substrate and filling them with materials such as silicon and silicon germanium (Column 4, Lines 1-10), as recited in claim 54 of the present invention. Cheng states that processing techniques such as immersion lithography can be used to process these semiconductor devices (Column 11, Lines 63-65).

It would have been obvious to one of ordinary skill in this art, at the time of invention by applicant, to have etched gate electrodes with a minimum dimension of 50 nm or less into the conductive layer, as suggested by Cheng, in the process of Hirayama ('400), Meagley and Chang because Cheng teaches that gate electrodes are often formed on semiconductor substrates and can be formed by immersion lithography. It also would have been obvious to have formed trenches in the dielectric layer and filled these with a conductor, as suggested by Cheng, because Cheng teaches that this is a common process for forming intricate semiconductor devices and can be formed by immersion lithography.

7. Claims 56, 58 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirayama (U.S. Patent Publication 2006/0141400) in view of Meagley (U.S. Patent Publication 2005/0084794), as applied to claims 23-30, 33, 34 and 61-65 above, and further in view of Lee (U.S. Patent Publication 2005/0266683).

The teachings of Hirayama ('400) and Meagley have been discussed in paragraph 2 above.

Hirayama ('400) and Meagley fail to disclose that a plasma treatment, a chemical treatment, or an ion implantation process can be used to treat the upper portion of the photoresist layer.

Lee discloses a photoresist that is used in lithography that can be modified by the following processes: chemical amplification, cross linking, chemical etching, deep ultraviolet treatment, ion implantation, plasma treatment, laser ablation, etc. (Paragraph 0034), as recited in claims 56, 58, and 59 of the present invention.

It would have been obvious to one of ordinary skill in this art, at the time of invention by applicant, to have used chemical amplification, ion implantation, plasma treatment, etc., as suggested by Lee, to form a barrier layer on a photoresist for the immersion lithography process of Hirayama ('400) and Meagley because Lee teaches that these processes work well at modifying a photoresist layer for a lithography process.

Response to Arguments

8. Applicant's arguments, with respect to the rejection of claims 23-60 on the ground of nonstatutory obviousness-type double patenting, have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

9. Applicant's amendments have overcome the rejection of claim 52 under 35 USC 112 2nd paragraph that was presented in the last Office Action. Examiner has withdrawn the rejection.

10. Applicant's arguments, filed 7/26/2007, with respect to the rejection of claims 23-60 under 35 USC 102(e) and 35 USC 103(a), have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, due to applicant's amendments, a new ground(s) of rejection is made in view of a newly found prior art reference.

The reference, Meagley, has been added to teach diffusion of the immersion fluid and the photoresist layer, as recited in independent claims 23 and 37 of the present invention. Dependent claims 24-34, 38-54, 56 and 58-60 are rejected for being dependent on rejected independent claims.

Newly added claims 61-65 have been rejected by Hirayama ('400) and Meagley because they teach immersion lithography processes with the upper portion of the photoresist layer being treated.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

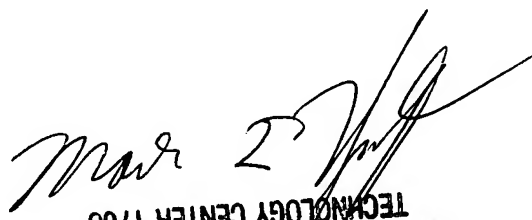
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brittany Raymond whose telephone number is 571-272-6545. The examiner can normally be reached on Monday through Friday, 8:00 a.m. - 4:30 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff can be reached on 571-272-1385. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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